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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/009,857	05/06/2002	Shinichi Yoshimura	113278-007	6313

29175 7590 08/16/2004

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EXAMINER

TRAN, TAM D

ART UNIT	PAPER NUMBER
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2676

DATE MAILED: 08/16/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/009,857

Applicant(s)

YOSHIMURA ET AL.

Examiner

Tam D Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 May 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 16-33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 16-33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Kobayashi et al. (USPN 6600160 B2), hereinafter simply Kobayashi.

2. In regard to claims 16, 22, 28, Kobayashi teaches a picture processing apparatus, comprising: a light receiving portion (Photoelectric conversion element, Photo diode) for generating an electric signal corresponding to an intensity of a received light; an amplifying portion (amplifying MOS transistor 22) for amplifying the electric signal generated by the light receiving portion; see Fig.1, see col.3 lines 52-55; a plurality of storing portions (capacitors C2), wherein each of the storing portions stores, as a current signal, the electric signal amplified by the amplifying portion; see Fig.1, Fig.4, Fig.13, col.10 lines 20-30; a load portion (source follower circuit read signal voltage with current amplified) for converting the current signal stored by each of the storing portions into a voltage signal; see col.5 lines 34-38; a bias portion (bias region where bias voltage (VDS) equal to pinch-off voltage) for supplying an offset current to an input of the load portion; see Fig.1, Fig.10, col.12 lines 1-5; a calculating portion (subtract circuit) for calculating an output signal of the load portion based on the voltage

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signal converted by the load portion; see Fig.10, see col.9 lines 16-25; and an outputting portion for outputting a calculated result of the calculating portion (signal output). See Fig.10.

3. In regard to claims 17, 23, 29, Kobayashi teaches a picture processing apparatus, wherein the plurality of storing portions store current signals corresponding to the intensity of light received in different time periods, and wherein the calculating portion performs a calculating process using voltage signals from at least two different time periods based on current signals extracted from at least two of the plurality of storing portions (Ct1, Ct2). See Fi.10, col.9 lines 16-44.

4. In regard to claims 18, 24, 30, Kobayashi teaches a picture processing apparatus, wherein the calculating process comprises at least one of addition, subtraction (subtraction processing), and comparison. See Fig.10, col.9 lines 16-25.

5. In regard to claims, 19, 25, Kobayashi teaches a picture processing apparatus, wherein the amplifying portion comprises a first mirror transistor and a second mirror transistor connected such that a gate electrode of the first mirror transistor faces a gate electrode of the second transistor (transistors 23, 22), thereby amplifying the current signal based on current mirror amplification, see Fig.1.

6. In regard to claims 20, 26, 33, Kobayashi teaches a picture processing apparatus, wherein each of the storing portions (capacitors) includes a current copier circuit for storing the current signal. See Fig.1, Fig.10.

7. In regard to claims 21, 27, 31, 32, Kobayashi teaches a picture processing apparatus, wherein the bias portion supplies an offset current to one of two current

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signals being compared by the calculating portion, the two current signals being supplied by two of the plurality of storage portions (capacitors). See Fig.10.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tam D. Tran** whose telephone number is

703-305-4196. The examiner can normally be reached on MON-FRI from 8:30 – 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Matthew Bella** can be reached on **703-308-6829**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service

Office whose telephone number is (703) 306-0377.

Tam Tran

TT
Examiner

Art unit 2676



MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600